PRODUCT	:	CAMERA MODULE
MODEL NO.	:	CM8487-B500SA-E
SUPPLIER	:	TRULY OPTO-ELECTRONICS LTD.
DATE	:	Oct 8,2015

CERT. No. 946535
ISO9001
TL9000

SPECIFICATION

Revision: 1.0

CM8487-B500SA-E

If there is no special request from customer, TRULY OPTO-ELECTRONICS LTD. will not reserve the tooling of the product under the following conditions:
1. There is no response from customer in two years after TRULY OPTO-ELECTRONICS LTD. submit the samples;
2. There is no order in two years after the latest mass production.
And correlated data (include quality record) will be reserved one year more after tooling was discarded.

TRULY OPTO-ELECTRONICS LTD.: CUSTOMER:

Approved by: Quality Assurance Department:_____ Technical Department:_____	Approved by:

REVISION RECORD

REV NO.	REV DATE	CONTENTS	REMARKS
1.0	2015-10-08	First release	Preliminary

CONTENTS

WRITTEN BY	CHECKED BY	APPROVED BY
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Key Information

Module No.		CM8487-B500SA-E
Module Size		8.50mm × 8.50mm × 4.96mm
Sensor Type		OV5640
Array Size	QSXGA	2592 × 1944
Power Supply	Analog	2.6~3.0V(2.8V typical)
	I/O	1.7~1.9V(1.8V typical)
	AF_VDD	2.8~3.3V
Lens Size and Structure		1/4 inch 4Plastic+IR
Lens F.NO		2.8
Lens View Angle		67.4°
IR Cutter		650nm
Object Distance		10cm~infinity
Input Clock Frequency		6~27MHz
Temperature Range	Operating	-20°C to 70°C
	Stable Image	0°C to 50°C
Output Formats		RAW RGB, RGB565/555/444, YUV422/420, YCbCr422, and compression
Maximum Image Transfer Rate		15fps@full resolution
Pixel Size		1.4μm × 1.4μm
Sensitivity		600mV/Lux-sec
Max S/N Ratio		36dB
Dynamic Range		68dB@8x gain
Sensor Power Requirement(Typ)	Active	140mA
	Standby	20μA
IC Package		71-pin CSP3
Substrate		FPC
Auto-Focus Type		VCM (Voice Coil Motor)
VCM Driver		Sensor internal driver
Package		Antistatic Plastic

Pin Assignment

No.	Name	Pin type	Description
1	STROBE	Output	Flash strobe output
2	AF_GND	Ground	VCM ground
3	AV_VDD	Power	VCM power ,2.8~3.3V
4	AGND	Ground	Analog ground
5	AVDD	Power	Analog power ,2.8V TYPE
6	DGND	Ground	Digital ground
7	SIOC	Input	SCCB input clock
8	SIOD	I/O	SCCB data
9	RESET	Input	Reset (active low with internal pull-up resistor)
10	NC	-	No connect
11	DGND	Ground	Digital ground
12	DGND	Ground	Digital ground
13	PWDN	Input	Power down (active high with internal pull-down resistor)
14	DGND	Ground	Digital ground
15	DGND	Ground	Digital ground
16	MDP2	Output	MIPI TX second data lane positive output
17	MDN2	Output	MIPI TX second data lane negative output
18	DGND	Ground	Digital ground
19	MCP	Output	MIPI TX clock lane positive output
20	MCN	Output	MIPI TX clock lane negative output
21	DGND	Ground	Digital ground
22	MDP1	Output	MIPI TX first data lane positive output
23	MDN1	Output	MIPI TX first data lane negative output
24	DGND	Ground	Digital ground
25	XCLK	Input	Clock input
26	DGND	Ground	Digital ground
27	NC	-	No connect
28	DOVDD	Power	I/O power ,1.8V TYPE
29	DGND	Ground	Digital ground
30	ID	Output	Camera identification, pulled high inside of module

Electrical Characteristics

1. Absolute Maximum Ratings

parameter		absolute maximum rating[a]
supply voltage (with respect to ground)[b]	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		±200 mA

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
b. for negative voltage with respect to ground, VDD-A (-4.5V), VDD-C (-3V), VDD-IO (-4.5V)

2. Functional temperature

parameter	range
operating temperature[a]	-20°C to +70°C junction temperature
stable image temperature[b]	0°C to +50°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range
b. image quality remains stable throughout this temperature range

3. DC Characteristics (-20°C < TA < 70°C)

symbol	parameter	min	typ	max	unit
power supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-D}[a]	supply voltage (digital core)	1.425	1.5	1.575	V
V_{DD-IO}	supply voltage (digital I/O)	1.71	1.8	3.0	V
internal DVDD short to DVDD, DVP output, AVDD = 2.8V, DOVDD = 2.8V					
I_{DD-A}	operating current 2592 x 1944 @ 15 fps JPG		30	40	mA
I_{DD-DO}			110	140	mA
I_{DD-A}	operating current 1080p @ 30 fps JPG		30	40	mA
I_{DD-DO}			100	130	mA
I_{DD-A}	operating current 720p @ 60 fps		32	42	mA
I_{DD-DO}			100	42	mA
I_{DD-A}	operating current 720 @ 30 fps YUV		32	40	mA
I_{DD-DO}			58	72	mA
I_{DD-A}	operating current VGA @ 30 fps		30	40	mA
I_{DD-DO}			58	72	mA
internal DVDD, EVDD short to DVDD, MIPI output, AVDD = 2.8V, DOVDD = 1.8V					
I_{DD-A}	operating current 2592 x 1944 @ 15 fps JPG		30	40	mA
I_{DD-DO}			110	140	mA
I_{DD-A}	operating current 2592 x 1944 @ 15 fps YUV		30	40	mA
I_{DD-DO}			100	130	mA
I_{DD-A}	operating current 1080p @ 30 fps JPG		30	40	mA
I_{DD-DO}			100	130	mA
I_{DD-A}	operating current 1080p @ 30 fps YUV		30	40	mA
I_{DD-DO}			90	115	mA
I_{DD-A}	operating current 720 @ 30 fps YUV		32	42	mA
I_{DD-DO}			54	70	mA
external DVDD, EVDD short to DVDD, DVP output, AVDD = 2.8V, DOVDD = 2.8V					
I_{DD-A}	operating current 2592 x 1944 @ 15 fps JPG		30	40	mA
I_{DD-D}			98	125	mA
I_{DD-DO}			9	12	mA

symbol	parameter	min	typ	max	unit
standby current					
$I_{DDS-SCCB}$			20	50	μA
$I_{DDS-PWDN}$			20	50	μA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs[b]					
V_{IL}	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}	SIOC and SIOD	1.26	1.8	3.0	V

a. using the internal DVDD regulator is strongly recommended for minimum power down current
b. based on DOVDD = 1.8V.

4. AC Characteristics

a. AC Characteristics (TA = 25°C, VDD-A = 2.8V)

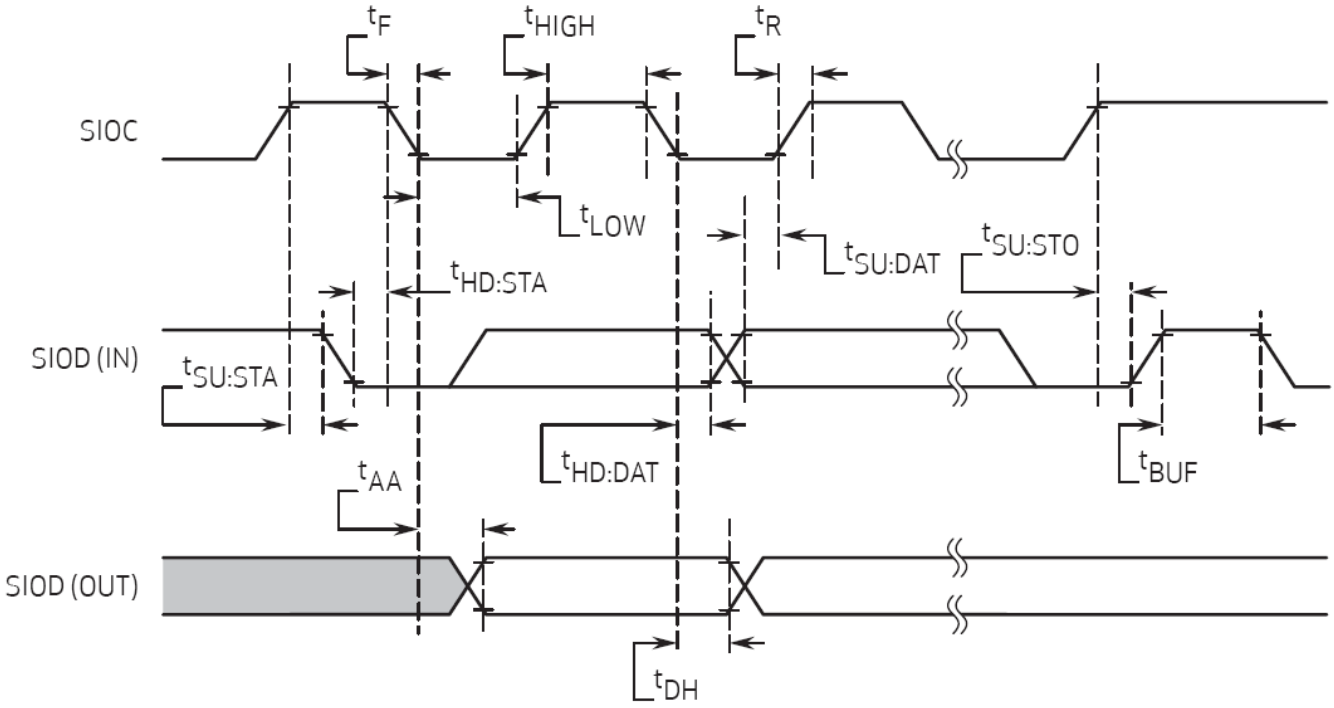
symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		30		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	settling time for hardware reset			<1	ms
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

b. Timing Characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)[a]	6	24	54	MHz
t_r, t_f	clock input rise/fall time[b]			5 (10[c])	ns
f_{PCLK}	parallel port output pixel clock		48[d]	96[e]	MHz

a. for input clock range 6~27 MHz, the OV5640 can tolerate input clock jitter up to 1ns, for input clock range to 54MHz, the OV5640 can tolerate input clock jitter up to 500 ps
b. if the PLL is bypassed, the delay from input clock to output clock is approximately 4~5 ns
c. if using the internal PLL
d. typical PCLK is 48 MHz when sensor output is smaller size (VGA YUV or below) or full size compression
e. 96 MHz is for sensor RAW data output at 15 fps or YUV output at 7.5 fps. For higher speeds such as 5 megapixel Y UV @ 15 fps, OmniVision recommends using the MIPI two-lane interface.

c. SCCB interface timing



SCCB interface timing specifications[a]

symbol	parameter	min	typ	max	unit
f_{SIOC}	clock frequency			400	KHz
t_{LOW}	clock low period	1.3			μs
t_{HIGH}	clock high period	0.6			μs
t_{AA}	SIOC low to data out valid	0.1		0.9	μs
t_{BUF}	bus free time before new start	1.3			μs
$t_{HD:STA}$	start condition hold time	0.6			μs
$t_{SU:STA}$	start condition setup time	0.6			μs
$t_{HD:DAT}$	data in hold time	0			μs
$t_{SU:DAT}$	data in setup time	0.1			μs
$t_{SU:STO}$	stop condition setup time	0.6			μs
t_R, t_F	SCCB rise/fall times			0.3	μs
t_{DH}	data out hold time	0.05			μs

a. SCCB timing is based on 400KHz mode

5. Format and frame rate

format	resolution	frame rate	scaling method	pixel clock
5 Mpixel	2592x1944	15 fps	full resolution (dummy 16 pixel horizontal, 8 lines) 2608x1952 with dummy	96/192 MHz
1280x960	1280x960	45 fps	subsampling in vertical and horizontal 1296x968 supports 2x2 binning	96/192 MHz
1080p	1920x1080	30 fps	cropping from full resolution 1936x1088 with dummy pixels	96/192 MHz
720p	1280x720	60 fps	cropping 2592x1944 to 2560x1440 subsampling in vertical and horizontal 1296x728 with dummy supports 2x2 binning	96/192 MHz
VGA	640x480	90 fps	subsampling from 1280x960 648x484 with dummy supports 2x2 binning	48/96 MHz
QVGA	320x240	120 fps	subsampling from 1280x960 324x242 with dummy supports 2x2 binning	24/48 MHz

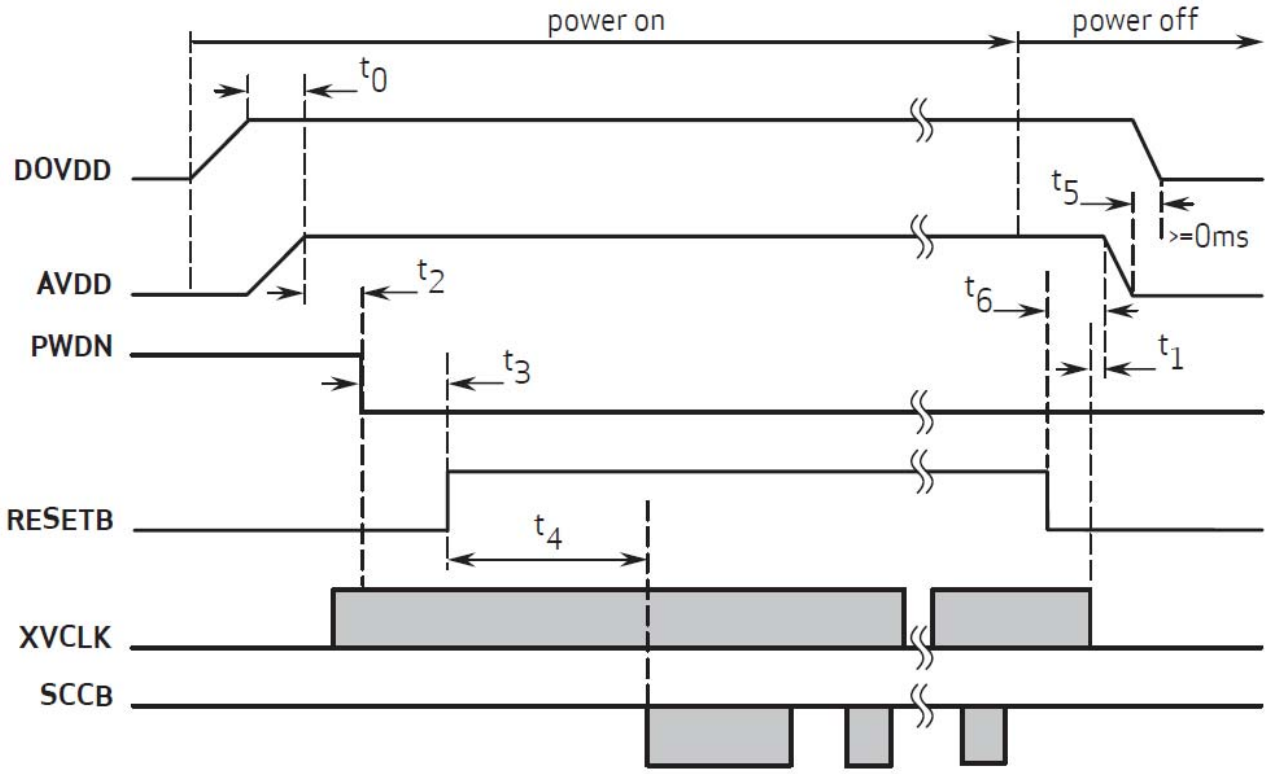
6. Power up sequence

Based on the system power configuration (1.8V or 2.8V for I/O power, using external DVDD or internal DVDD, requiring access to the I2C during power up period or not), the power up sequence will differ. If 1.8V is used for I/O power, using the internal DVDD is preferred. If 2.8V is used for I/O power, due to a high voltage drop at the internal DVDD regulator, there is a potential heat issue. Hence, for a 2.8V power system, OmniVision recommends using an external DVDD source. Due to the higher power down current when using an external DVDD source, OmniVision strongly recommends cutting off all powers, including the external DVDD, when the sensor is not in use in the case of 2.8V I/O and external DVDD.

a. Power up with internal DVDD

For powering up with the internal DVDD and I2C access during the power ON period, the following conditions must occur:

1. When DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable.
2. PWDN is active high with an asynchronized design (does not need clock).
3. PWDN pin tied to digital ground if it is not controlled.
4. If PWDN pin is controlled as below, for PWDN to go low, power must first become stable (AVDD to PWDN ≥ 5 ms).
5. RESETB is active low with an asynchronized design.
6. Master clock XVCLK should provide at least 1 ms before host accesses the sensor's registers.
7. Host can access I2C bus (if shared) during entire period. 20ms after RESETB goes high, host can access the sensor's registers to initialize sensor.



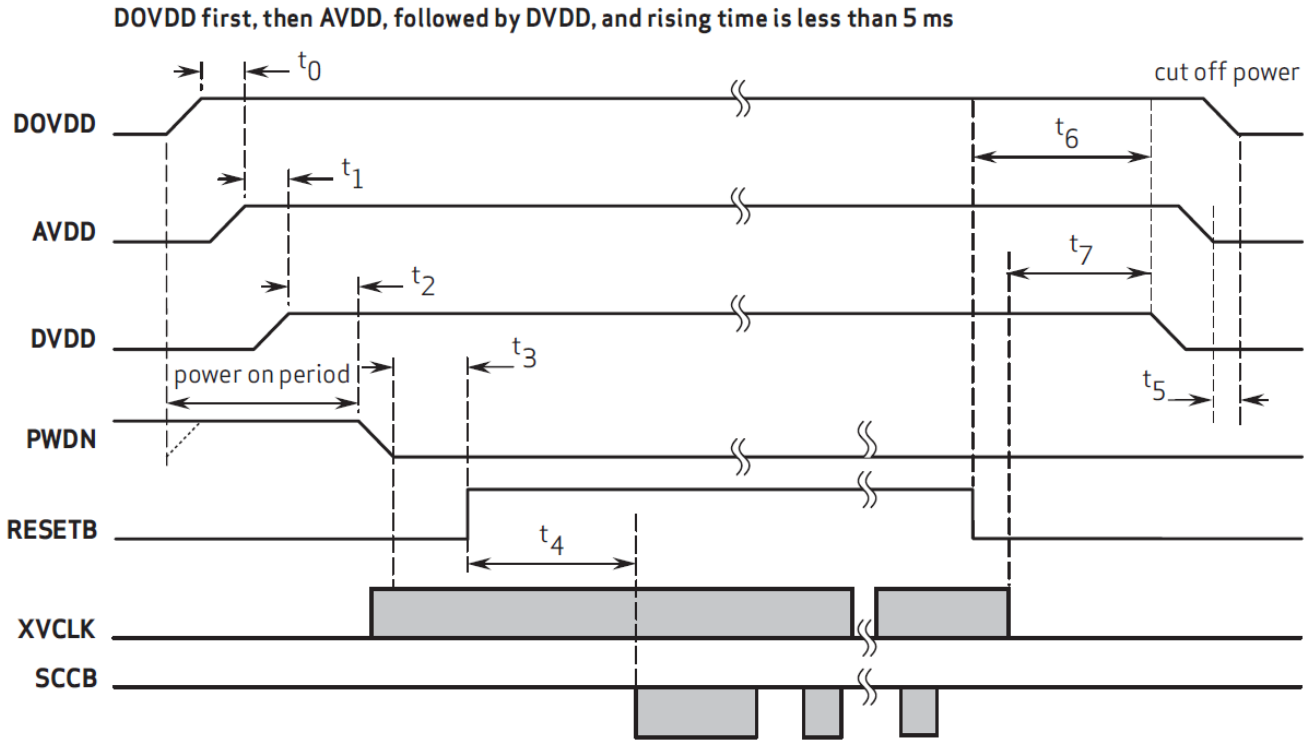
Note:

t0 ≥ 0ms: delay from DOVDD stable to AVDD stable, it is recommended to power up AVDD shortly after DOVDD has been powered up.
t1 ≥ 0ms: delay from XVCLK off to AVDD off.
t2 ≥ 5ms: delay from AVDD stable to sensor power up stable, PWDN can be pulled low after this point, XVCLK can be turned on after power on.
t3 ≥ 1ms: delay from sensor power up stable to RESETB pull up.
t4 ≥ 20ms: delay from RESETB pull high to SCCB initialization.
t5 ≥ 0ms: delay from AVDD off to DOVDD off.
t6 ≥ 0ms: delay from RESETB pull low to AVDD off.

b. Power up with external DVDD source

For powering up with an external DVDD source and I2C access during the power ON period, the following conditions must occur:

1. When DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable.
2. When AVDD and DVDD are turned ON, make sure AVDD becomes stable before DVDD becomes stable.
3. PWDN is active high with an asynchronized design (does not need clock), PWDN pin tied to digital ground if it is not controlled.
4. For PWDN to go low, power must first become stable (DVDD to PWDN ≥ 5 ms)..
5. All powers are cut off when the camera is not in use (power down mode is not recommended.
6. RESETB is active low with an asynchronized design.
7. Master clock XVCLK should provide at least 1 ms before host accesses the sensor's registers.
8. Host can access I2C bus (if shared) during entire period. 20ms after RESETB goes high, host can access the sensor's registers to initialize sensor.



Note:

t0 ≥ 0 ms: delay from DOVDD stable to AVDD stable, it is recommended to power up AVDD shortly after DOVDD has been powered up
t1 ≥ 0 ms: delay from AVDD stable to DVDD stable
t2 ≥ 5 ms: delay from DVDD stable to sensor power up stable
t3 ≥ 1ms: delay from sensor power up stable to RESETB pull up
t4 ≥ 20ms: delay from RESETB pull high to SCCB initialization
t5 ≥ 0ms:delay from AVDD off to DOVDD off
t6 ≥ 0ms: delay from RESETB pull low to DVDD off
t7 ≥ 0ms: delay from XVCLK off to DVDD off

7. Reset

The OV5640 sensor includes a RESETB pin that forces a complete hardware reset when it is pulled low (GND). The OV5640 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register 0x3008[7] to high.

Manually applying a hard reset upon power up is required even though on-chip reset is included. The hard reset is active low with an asynchronized design. The reset pulse width should be greater than or equal to 1 ms.

8. Hardware and software standby

Two suspend modes are available for the OV5640:
- hardware standby
- SCCB software standby

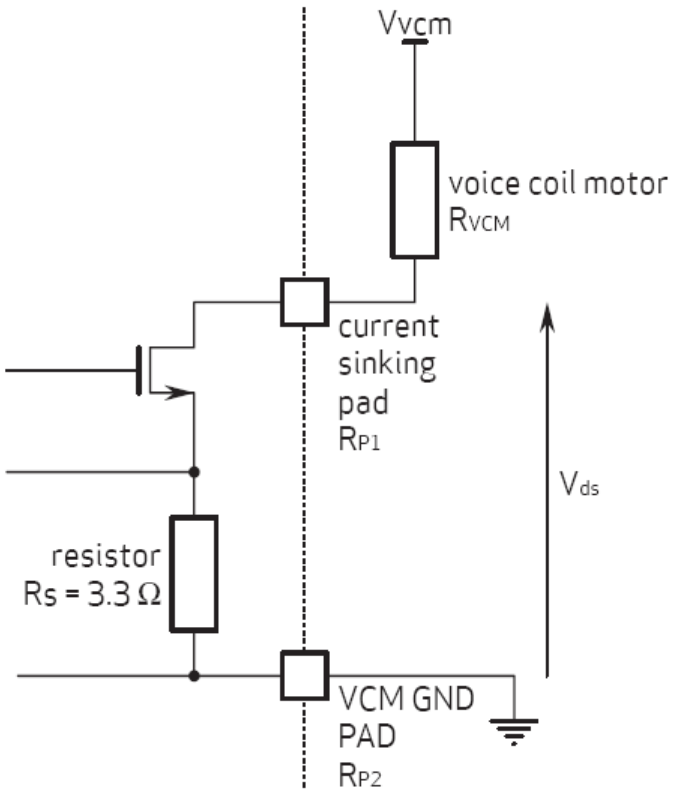
To initiate hardware standby mode, the PWDN pin must be tied to high (while in MIPI mode, set register 0x300E[4:3] to 2'b11 before the PWDN pin is set to high). When this occurs, the OV5640 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software standby through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

9. VCM driver

The OV5640 support auto focus control (AFC) with embedded AF VCM driver.

VCM block diagram



The maximum SINK current can be estimated as:

- ISINK = (Vvcm - Vds) / (Rs + Rvcm + Rp1 + Rp2)
- Vds is the transistor headroom
- Rp1 and Rp2 are the resistance in the current path
- RVCM is the resistance of the voice coil motor.

The OV5640 VCM driver is a single 10-bit DAC with 100 mA output current sink capability. It is designed for linear control of the VCM. The DAC is controlled via the SCCB interface with clock rates up to 400 Hz. The OV5640 VCM driver provides three types of output current control modes that allow users to adjust transient response of the sinking current.

The OV5640 VCM driver uses 4 bits (S3, S2, S1, and S0) to control the output current response.

1. S[3:0] = X000: Directly jump mode: code directly jumps to target code. Output current transient response time (see table 3-2.)

2. S[3:0] = 0001 to 0111: Single step mode: code increases/decreases by a single step. Single step time durations are 50µs, 100µs, 200µs, 400µs, 800µs, 1600µs, and 3200µs, which are controlled by S2, S1, and S0 (see table 3-4.)

3. S[3:0] = 1001 to 1111: Multi-code steps mode: Code increases/decreases in multi-code steps. If the target code and the current code have a difference larger than 128, the 64-code step is applied first. When the difference in between target and current codes is no more than 128 but larger than 16, the 16-code step is used. When the difference is less than 16, it will directly jump to the target code. Single step time options are 50µs, 100µs, 200µs, 400µs, 800µs, 1600µs, and 3200µs, which are controlled by S2, S1, and S0, (see table 3-5.)

table 3-2 VCM driver control

function	register	description
current transient response control	0x3602	Bit[3:0]: Current transient response control x000: mode 0 0001~0111: mode 1 1001~1111: mode 2
10-bit DAC code	0x3603[5:0], 0x3602[7:4]	0x3603[5:0]: D[9:4] 0x3602[7:4]: D[3:0]
clock divider	0x3605[3:0], 0x3606[7:0]	divide external clock to obtain a 20 KHz clock for VCM control block VCM control clock = external clock / Rdiv[11:0]

table 3-3 VCM control registers

address	register name	default value	R/W	description
0x3603	VCM[15:8]	0x01	RW	Bit[7]: PD Bit[5:0]: D[9:4]
0x3602	VCM[7:0]	0x50	RW	Bit[7:4]: D[3:0] Bit[3]: S3 Bit[2:0]: S[2:0]
0x3605	SLEW[11:8]	0x46	RW	Bit[3:0]: Rdiv[11:8]
0x3604	SLEW[7:0]	0x05	RW	Bit[7:0]: Rdiv[7:0]
0x3606	VCM CURRENT	0x00	RW	Bit[2:0]: VCM output current control 000: 0.71 * Id 001: 0.77 * Id 010: 0.83 * Id 011: 0.91 * Id 100: 1.00 * Id 101: 1.11 * Id 110: 1.25 * Id 111: 1.43 * Id

table 3-4 single step mode

mode	S3	S2	S1	S0	single step transition time	full scale transition time (1023 steps)
single step mode	0	0	0	1	50μs	51.15ms
	0	0	1	0	100μs	102.3ms
	0	0	1	1	200μs	204.6ms
	0	1	0	0	400μs	409.2ms
	0	1	0	1	800μs	818.4ms
	0	1	1	0	1600μs	1.637s
	0	1	1	1	3200μs	3.274s

table 3-5 multi-code step mode

mode	S3	S2	S1	S0	single step transition time	full scale transition time (22 steps)[a]
single step mode	1	0	0	1	50μs	1.1ms
	1	0	1	0	100μs	2.2ms
	1	0	1	1	200μs	4.4ms
	1	1	0	0	400μs	8.8ms
	1	1	0	1	800μs	17.6ms
	1	1	1	0	1600μs	35.2ms
	1	1	1	1	3200μs	70.4ms

a. a full scale transition includes fourteen 64-code steps, seven 16-code steps and one directly jump step.

figure 3-4 1/4 to 3/4 scale settling time (directly jump mode, VDD = 3.0V)

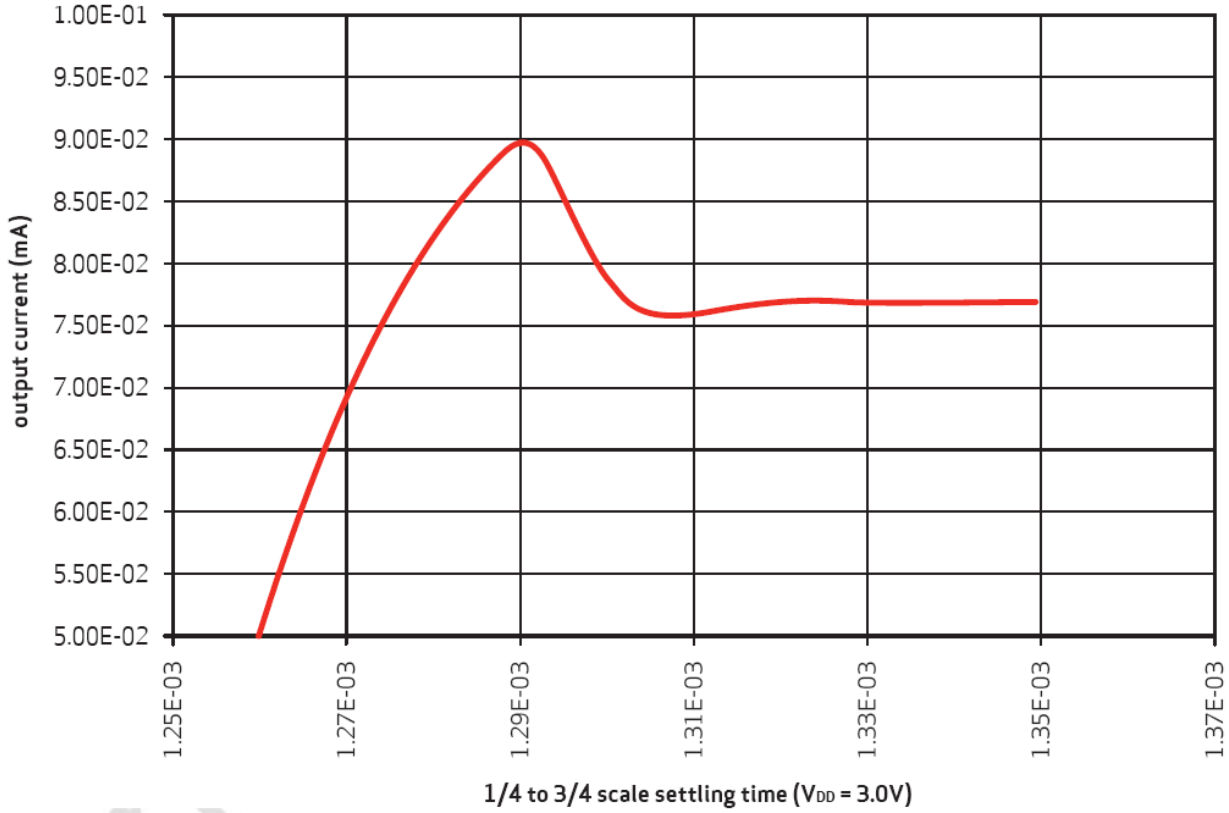
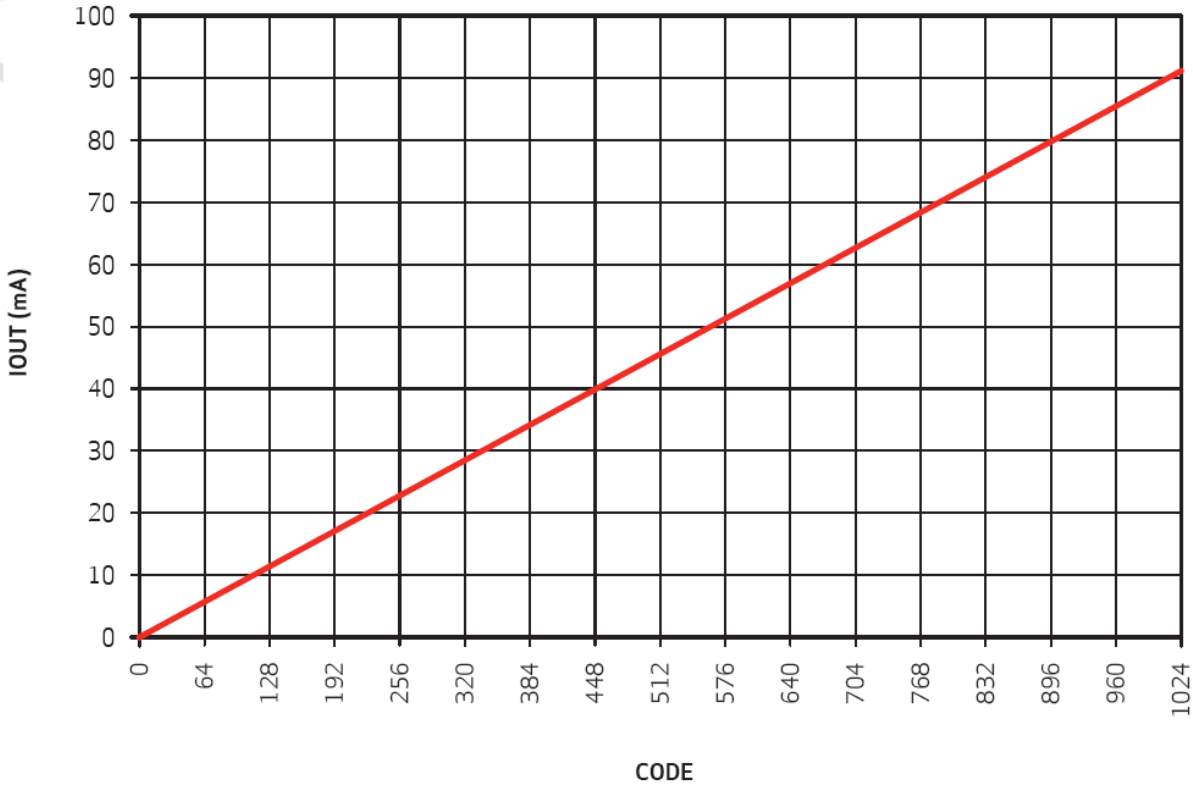


figure 3-5 sink current vs. code (VDD = 3.0V, reg 0x30A5 = 0x05, VCM resistance = 23ohms)

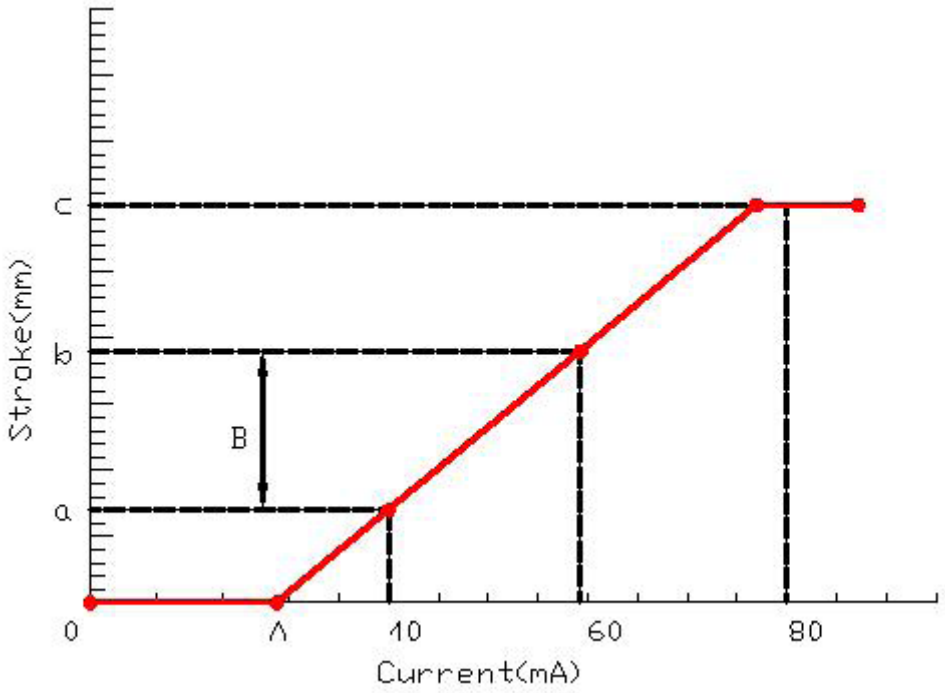


Note: For more information of sensor please refer to the OV5640 specification.

10. VCM specification

NO.	Item	Condition	Specification
1	Motor Size	With alignment wall	8.5×8.5×4.60 mm
2	Rated Current		≤80mA
3	Coil Resistance		23.5±10%Ω
4	Rated Stroke	Under 80mA input current	≥0.20mm

Performance Diagram

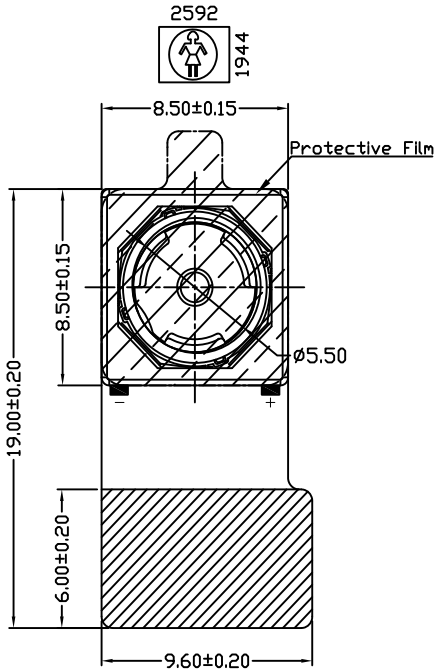


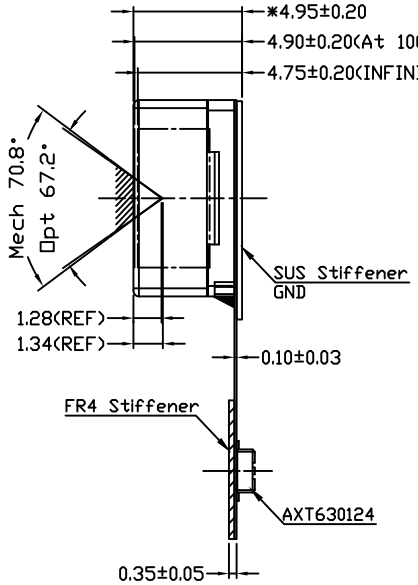
Mechanical Drawing

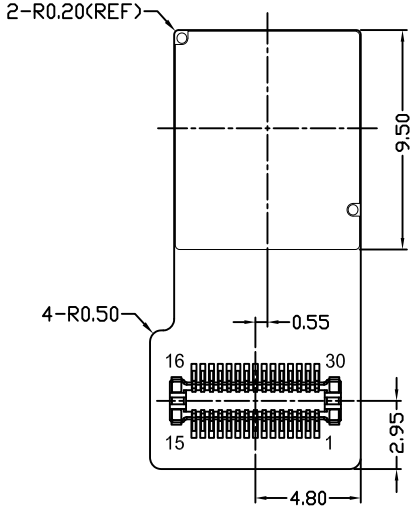
Customer No.:

CM8487-B500SA-E Camera Module

Hazardous Substance Management Standards
- ☐ EU RoHS
- ■ EU RoHS + Halogen-Free
- ☐ _____Hazardous Substance Management Standards Ver. ___







30PIN DESCRIPTION

PIN NO	NAME
1	STROBE
2	AF_GND
3	AF_VDD_2V8
4	AGND
5	AVDD_2V8
6	DGND
7	SIOC
8	SIOD
9	RESET
10	NC
11	DGND
12	DGND
13	PWDN
14	DGND
15	DGND
16	MDP2
17	MDN2
18	DGND
19	MCP
20	MCN
21	DGND
22	MDP1
23	MDN1
24	DGND
25	XCLK
26	DGND
27	NC
28	DOVDD_1V8
29	DGND
30	ID

主要参数(Module Specification)	
焦距(EFL)	3.43mm
光圈(F.NO)	2.8
视场角(View Angle)	67.2°
畸变(TV-Distortion)	≤ 2 %
景深(Focusing Range)	10 cm~Infinity
感光芯片(Chip Type)	OV5640
象素(Array Size)	5.0M
镜头类型(lens Size)	1/4 INCH 4P+IR

Note:
1.* IS Critical Dimension
2.Power Supply:
AVDD------2.6V to 3.0V (2.8V typical)
DOVDD-----1.7V to 1.9V (1.8V typical)
3.Pin#30(ID) is pulled high inside of module

Actuator Specification

Type	VCM Parameter
Control Mode	IIC
Supply Voltage	2.8V~3.3V
Coil Resistance	17±15%ohm
Rated Current	no more than 100mA

CUSTOMER APPROVE		AMEND			摄像模组	TRULY OPTO-ELECTRONICS LTD.		
Mechanical	Electrical	△			TOLERANCE: DECIMAL .x ± .30 .xx ± .20 ∠ ± 1/4	PRODUCT NO. CM8487-B500SA-E	DRAW NO. 标准品	REV A
		△				DWN Allen 20150909	DSN Allen 20150909	
		△				CHKD Weiyx 20150909	APPD Bruce 20150909	
		△				NOT IN SCALE	UNIT mm	SHEET: 1/1
		NO.	CONTENT	DATE				

Appearance Specification

NO.	Item	Standard	Importance Class
1	Top side of Lens	1.No obvious impurity and No feeling nick defect and oil impurity on the surface of lens within 1/2 area; 2.there is no chip or crack on the lens at another 1/2 area	A
2	Screw glue	Normally screw glue shall be symmetrical distributed around lens circle side. Particular circs, glue distribution must not disturb customer's assembly operation.	A
3	Sealed glue	Sealed glue distributing between holder and FPC must be symmetrical and smooth. Not allow glue leakage and asymmetric thickness. After holder assembly, the thickness distance between one side and its opposite side shall be less than 0.2mm. Excess glue over the holder shall not make the outside dimension be out of control.	A
4	FPC/PCB	Edge defect limitation: width≤1/2H (H is minimum.)、length≤1mm、defect numbers per edge≤2(No tearing gap inby edge for FPC); Edge outshoot limitation (width≤ 0.3mm, length≤1mm). No obvious impurity and crease on the surface. If there was shield film on the surface, the spot size of the film shall be less than 0.3mm×1mm and no line is exposed. If it was not be cleaned and did not influence the total thickness, it would be permitted. Label and mark shall be clear enough to be discerned.	A
5	Connector	No dust, fingerprint, and not allows to turning colors, distortion; Solder must be well; No open circuit or short circuit.	A
6	Stiffener	Holder anchor pole length overtopping the steel plate shall be less than 0.2mm. No dust, rust and deep scratch on the steel surface without Double coated tapes.	B
7	Protective film	No dust in the glue side. Not allows to float or drop.	B

Remark:

1. The definition of the appearance importance class

A：The defect can be found in the finished product, or have obvious visual differences from good products, such as crack, defect and dust, or influence image quality, or are appointed by the customer. We will emphasize these items and check all products.

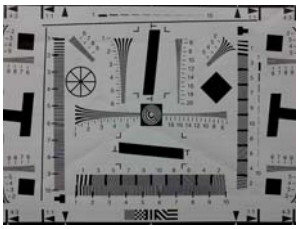
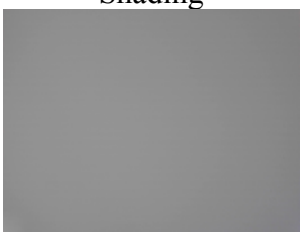
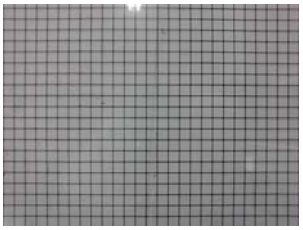
B：The defect can be found in the finished product and has visual difference from the good one, but will not affect customer's aesthetic judgement. Or the defect can not be found in the finished product and will not generate functional problem, but will slightly influence sequential manufacture process or condition. We will supervise these items in the manufacturing process and check products selectively.

C：Check method: distance 30cm, visual vertical or 45°reflection.

2. Sampling standard

Referenced standard: GB/T 2828.1-2003/ISO 2859-1:1999 and ANSI/ASQC.4-1993 Ⅱ

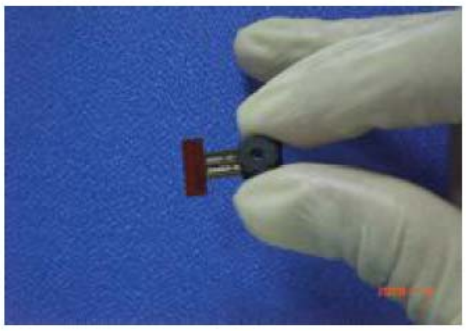
Image Specification

NO.	Item	Standard
1	TV Line 	Center≥1200 0.7 viewing field ≥900
2	Shading 	The Brightness of 90% viewing area ≥60% of center Brightness (Lens correction Shading [Turn on])
3	Blemish 	Full screen IC Blemish: Contrast>10%, Pixel number≤4*5 IR Blemish: Contrast>1.0%, Pixel number≤100*100
4	Distortion 	TV Distortion≤2%

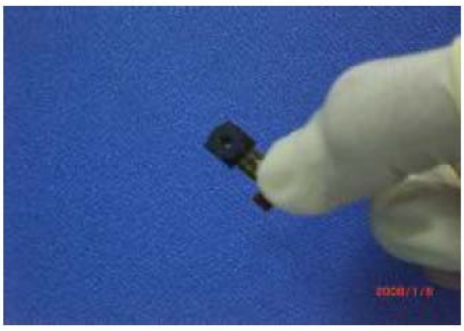
Precautions for Using CCM Modules

Handing Precautions

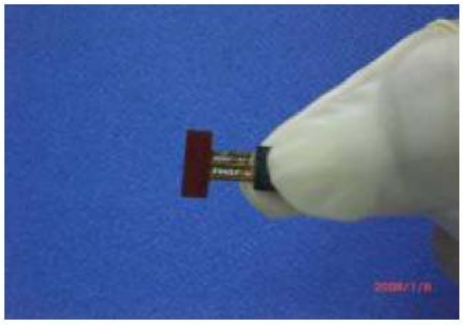
—DO NOT try to open the unit enclosure as there is no user-serviceable component inside. To prevent damage to the camera module by electrostatic discharge, handling the camera module only after discharging all static electricity from yourself and ensuring a static-free environment for the camera module.
—DO NOT touch the top surface of the lens.
—DO NOT press down on the lens.
—DO NOT try to focus the lens.
—DO NOT put the camera module in a dusty environment.
—To reduce the risk of electrical shock and damage to the camera module, turn off the power before connect and disconnect the camera module.
—DO NOT drop the camera module more than 60 cm onto any hard surface.
—DO NOT expose the camera module to rain or moisture.
—DO NOT expose the camera module to direct sunlight.
—DO NOT put the camera module in a high temperature environment.
—DO NOT use liquid or aerosol cleaners to clean the lens.
—DO NOT make any charges or modifications to the camera module.
—DO NOT subject the camera module to strong electromagnetic field.
—DO NOT subject the camera module to excessive vibration or shock.
—DO NOT impact or nip the camera module with speculate things
—DO NOT alter, modify or change the shape of the tab on the metal frame.
—DO NOT make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
—DO NOT damage or modify the pattern writing on the printed circuit board.
—Absolutely DO NOT modify the zebra rubber strip (conductive rubber) or heat seal connector
—Except for soldering the interface, DO NOT make any alterations or modifications with a soldering iron.
—DO NOT twist FPC of CCM.



Correct



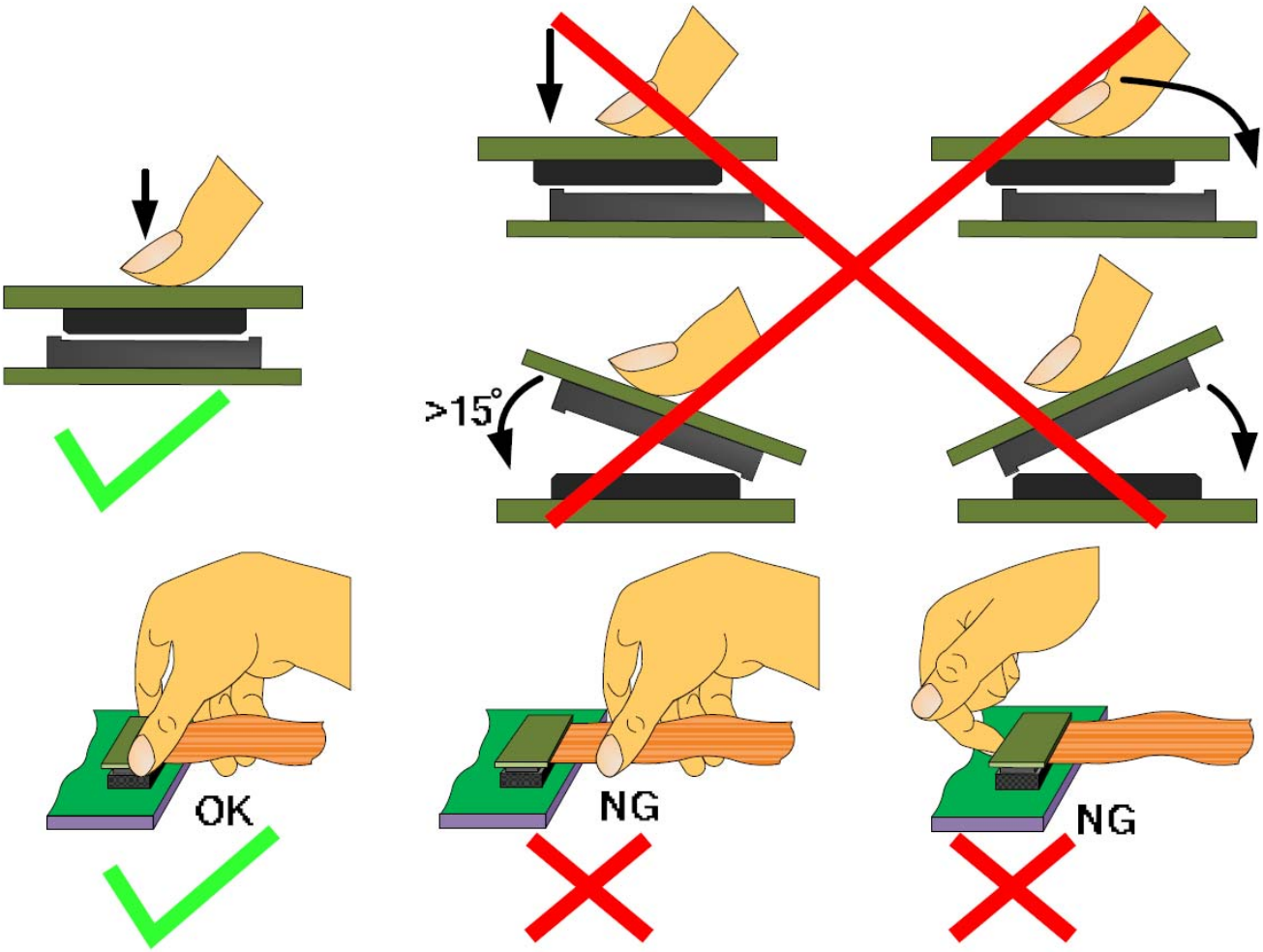
Incorrect



Incorrect

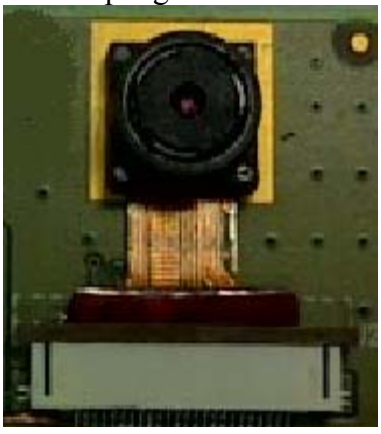
Precaution for assemble the module with BTB connector:

Please note the position of the male and female connector position, don't assemble or assemble like the method which the following picture shows



Precaution for assembling the module to terminal unit

The temperature of running module is high base on the high-integrated sensor. In order to enhance the heat dissipation and reduce the noise infection from high temperature, TRULY recommend that the module's backside should be touched with rigid material directly, like as PCB or metal. If necessary, it's recommended the module backside is affixed with the materials which can transfer heat, like as electric-fabric, electric-adhesive, or electric-sponge.



Precaution for soldering the CCM:

	Manual soldering	Machine drag soldering	Machine press soldering
Non-RoHS product	290°C ~350°C Time: 3-5s	330°C ~350°C Speed: 4-8mm/s	300°C ~330°C Time: 3-6s Press: 0.8~1.2Mpa
RoHS product	340°C ~370°C Time: 3-5s	350°C ~370°C Speed: 4-8mm/s	330°C ~360°C Time: 3-6s Press: 0.8~1.2Mpa

(1) If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the lens surface with a cover during soldering to prevent any damage due to flux spatters.
(2) The CCM module and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

Other precautions

For correct using please refer to the relative criterions of electronic products.

Limited Warranty

Unless agreed between TRULY and customer, TRULY will replace or repair any of its CCM modules which are found to be functionally defective when inspected in accordance with TRULY CCM acceptance standards for a period of one year from date of shipments. Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of TRULY limited to repair and/or replacement on the terms set forth above. TRULY will not being responsible for any subsequent or consequential events.

Return CCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are:

-Holder is apart from module.
-Holder or Connector is anamorphic.
-Connector is turn-up.
-FPC is lacerated or discon-nexion, and so on.

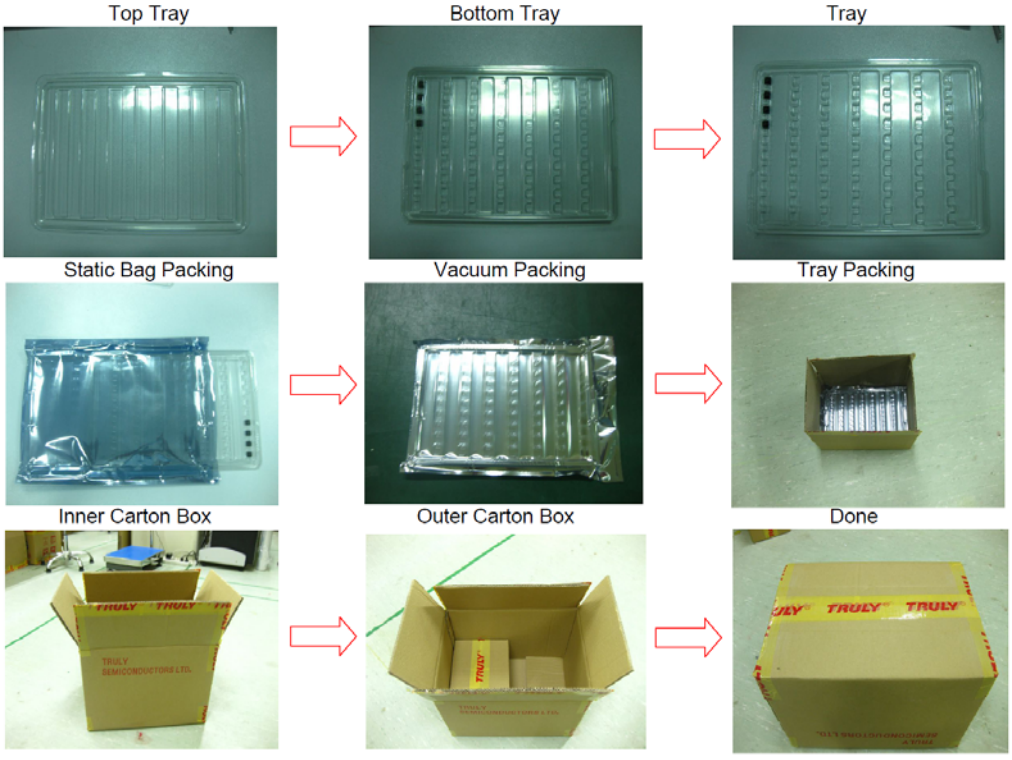
Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet, conductors and terminals.

Package Specification

Packaging Design One

Product No.	CM8487-B500SA-E	Release date	
Product name	Compact Camera Module	Releaser	
Supplier	TRULY OPTO-ELECTRONICS LTD.	Recycle	☐YES ■NO
Quantity/ each box	TBD	Material for box	■paper ☐plastic
Outer carton box size	405mm*290mm*290mm	Box type	■new ☐update
Quantity / inner box * Quantity / outer box	TBD		

Packing Standards:



There are TBD modules in each plastic plate.

There are TBD modules in each inner carton box.

There are 4 inner carton boxes in each outer carton box.

Requirements of outer carton box :

1. Weight(Max): TBD Kg
2. Height (Max): 0.29 M
3. Prohibition: Box made by log

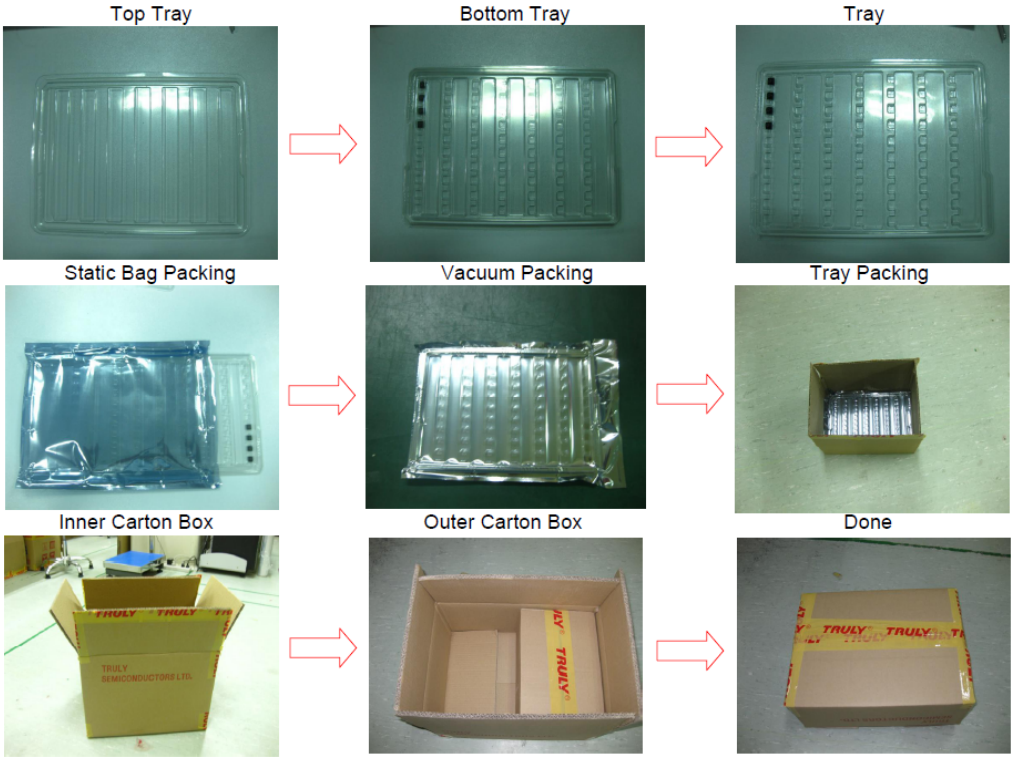
Material for Plastic tray

It is made of antistatic polystyrene which has no chemical pollution. Surface resistivity : 10^6 ohm/sq

Packaging Design Two

Product No.	CM8487-B500SA-E	Release date	
Product name	Compact Camera Module	Releaser	
Supplier	TRULY OPTO-ELECTRONICS LTD.	Recycle	☐YES ■NO
Quantity/ each box	TBD	Material for box	■paper ☐plastic
Outer carton box size	405 mm *290 mm *170 mm	Box type	■new ☐update
Quantity / inner box * Quantity / outer box	TBD		

Packing Standards:



There are TBD modules in each plastic plate.

There are TBD modules in each inner carton box.

There are 2 inner carton boxes in each outer carton box.

Requirements of outer carton box :

4. Weight(Max): TBD Kg
5. Height (Max): 0.17 M
6. Prohibition: Box made by log

Material for Plastic tray

It is made of antistatic polystyrene which has no chemical pollution. Surface resistivity : 10^6 ohm/sq

Prior Consult Matter

1.①For Truly standard products, we keep the right to change material, process for improving the product property without notice on our customer.
②For OEM products, if any change needed which may affect the product property, we will consult with our customer in advance.
2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.

Factory Contact Information

FACTORY NAME: TRULY OPTO-ELECTRONICS LTD.
FACTORY ADDRESS: Truly Industrial Area, ShanWei City, GuangDong, China
URL: http://www.trulyopto.com